IN THE CLAIMS:

Please amend claims 13 and 14 as follows.

1. (Canceled)

2. (Previously Presented) The phase adjustment circuit of claim 13, wherein the clock proliferators generates the plurality of clock signals by delaying the first clock signal by different amounts.

3. (Original) The phase adjustment circuit of claim 2, wherein the clock proliferators comprises a cascaded plurality of delay elements.

4. (Previously Presented) The phase adjustment circuit of claim 13, further comprising:

an external input terminal for input of the selection signal; and

an external output terminal for output of the detection signal.

5. (Previously Presented) The phase adjustment circuit of claim 13, further comprising:

an externally writable register that stores the selection signal and supplies the selection signal to the clock selector; and

an external output terminal for output of the detection signal.

6. (Previously Presented) The phase adjustment circuit of claim 13, wherein the phase difference detector comprises:

a first flip-flop that latches and outputs the state of the second clock signal at rising edges of the selected clock signal;

a second flip-flop that latches and outputs the state of the second clock signal at falling edges of the selected clock signal; and

a logic circuit that performs a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal.

7. (Original) The phase adjustment circuit of claim 6, wherein the first clock signal has a lower frequency than the second clock signal.

8. (Previously Presented) The phase adjustment circuit of claim 13, wherein the phase difference detector comprises:

a first-flop that latches and outputs the state of the selected clock signal at rising edges of the second clock signal;

a second flip-flop that latches and outputs the state of the second clock signal at falling edges of the selected clock signal; and

a logic circuit that performs a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal.

9. (Original) The phase adjustment circuit of claim 8, wherein the first clock signal has a higher frequency than the second clock signal.

10. (Previously Presented) The phase adjustment circuit of claim 13, further comprising a selection signal generator that receives the detection signal and generates the selection signal.

11. (Original) The phase adjustment circuit of claim 10, wherein the selection signal generator cyclically increases or decreases the selection signal within a certain range of values while the detection signal indicates that the predetermined condition is not satisfied, and holds the selection signal constant while the detection signal indicates that the predetermined condition is satisfied.

12. (Previously Presented) The phase adjustment circuit of claim 10, wherein the selection signal generator comprises:

a register that stores the value of the selection signal;

an adder that adds a fixed value to the value stored in the register to generate a sum value; and

a selector that receives the value stored in the register and the sum value, selects the value stored in the register when the detection signal indicates that the

predetermined condition is satisfied, selects the sum value when the detection signal indicates that the predetermined condition is not satisfied, writes the selected value in the register, and supplies the selected value to the clock selector as the selection signal.

13. (Currently Amended) A phase adjustment circuit that receives a first pair of clock signals and outputs a second pair of clock signals with phases satisfying a predetermined condition to a central processing unit, comprising:

a clock proliferator that receives a first clock signal and generates a plurality of clock signals therefrom;

a clock selector that receives said plurality of clock signals from the clock proliferator, selects one of the received plurality of clock signals in accordance with a selection signal, and outputs ~~the~~ a selected clock signal; and

a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied;

the first clock signal and the second clock signal constituting the first pair of clock signals;

the second clock signal and the selected clock signal constituting the second pair of clock signals;

wherein the selected clock signal has a lower frequency than the second clock signal, and the predetermined condition specifies that all rising and falling edges of the selected clock signal occur while the second clock signal is high.

14. (Currently Amended) A phase adjustment circuit that receives a first pair of clock signals and outputs a second pair of clock signals with phases satisfying a predetermined condition to a central processing unit, comprising:

a clock proliferator that receives a first clock signal and generates a plurality of clock signals therefrom;

a clock selector that receives said plurality of clock signals from the clock proliferator, selects one of the received plurality of clock signals in accordance with a selection signal, and outputs ~~the~~ a selected clock signal; and

a phase difference detector that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputs a detection signal indicating whether the predetermined condition is satisfied;

the first clock signal and the second clock signal constituting the first pair of clock signals;

the second clock signal and the selected clock signal constituting the second pair of clock signals;

wherein the selected clock signal has a higher frequency than the second clock signal, and the predetermined condition specifies that all rising and falling edges of the second clock signal occur while the selected clock signal is high.

15. (Previously Presented) The phase adjustment circuit of claim 14, wherein the clock proliferators generates the plurality of clock signals by delaying the first clock signal by different amounts.

16. (Previously Presented) The phase adjustment circuit of claim 15, wherein the clock proliferators comprises a cascaded plurality of delay elements.

17. (Previously Presented) The phase adjustment circuit of claim 14, further comprising:

an external input terminal for input of the selection signal; and

an external output terminal for output of the detection signal.

18. (Previously Presented) The phase adjustment circuit of claim 14, further comprising:

an externally writable register that stores the selection signal and supplies the selection signal to the clock selector; and

an external output terminal for output of the detection signal.

19. (Previously Presented) The phase adjustment circuit of claim 14, further comprising a selection signal generator that receives the detection signal and generates the selection signal.

20. (Previously Presented) The phase adjustment circuit of claim 19, wherein the selection signal generator cyclically increases or decreases the selection signal within a certain range of values while the detection signal indicates that the predetermined condition is not satisfied, and holds the selection signal constant while the detection signal indicates that the predetermined condition is satisfied.

21. (Previously Presented) The phase adjustment circuit of claim 19, wherein the selection signal generator comprises:

a register that stores the value of the selection signal;

an adder that adds a fixed value to the value stored in the register to generate a sum value; and

a selector that receives the value stored in the register and the sum value, selects the value stored in the register when the detection signal indicates that the predetermined condition is satisfied, selects the sum value when the detection signal indicates that the predetermined condition is not satisfied, writes the selected value in the register, and supplies the selected value to the clock selector as the selection signal.